Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit for controlling a fusing system, comprising:

a timing circuit which, in response to at least one input, is configured to produce a timing control signal;

an averaging circuit configured to receive the timing control signal from the timing circuit and to average the signal to produce an averaged signal;

a frequency modulation circuit configured to receive the averaged signal from the averaging circuit and to generate a train of pulses which varies with a voltage of the averaged signal; and

a switch driver circuit which is configured to be responsive to the pulse train from the frequency modulation circuit and to drive a power supply switching circuit with a timing to apply a smoothly changing alternating current to the fusing system.

2. (Original) A circuit as set forth in claim 1, further comprising an opto-isolator interposed between the timing circuit and the averaging circuit and configured to isolate the timing circuit from the voltage of an alternating current supplied by the switch driver circuit to the fusing system.

3. (Original) A circuit as set forth in claim 1, wherein the timing circuit comprises a circuit which is configured to produce a series of pulses the width of which are varied in accordance with a predetermined control.

4. (Original) A circuit as set forth in claim 3, wherein the predetermined control comprises a phase angle control.

5. (Original) A circuit as set forth in claim 3, wherein the predetermined control comprises integral half cycle control.

6. (Original) A circuit as set forth in claim 3, wherein the predetermined control comprises a hysteresis control wherein the pulse width of each of the pulses corresponds to a predetermined length of time.

7. (Currently Amended) A circuit as set forth in claim 1, wherein [[the]] a modulation circuit arrangement comprises a pulse width modulation (PWM) circuit which receives [[the]] a voltage signal output from the averaging circuit and produces a pulse train having a duty cycle which varies with the voltage signal output from the averaging circuit.

8. (Currently Amended) A circuit as set forth in claim 7 [[1]], wherein the modulation circuit arrangement comprises a voltage controlled oscillator and resetable monostable multivibrator serially connected to the oscillator.

9. (Currently Amended) A circuit as set forth in claim 7 [[1]], wherein the modulation circuit arrangement comprises an oscillator, a ramp generator serially connected to the oscillator and a comparator connected to the averaging circuit and the ramp generator.

10. (Original) A circuit as set forth in claim 1, wherein the timing circuit is a phase angle responsive circuit configured to produce pulses having a width corresponding to the time interval between the alternating current reaching maximum and minimum values.

11. (Original) A circuit as set forth in claim 1, wherein the timing circuit is an integral half cycle circuit configured to produce pulses the width of which vary with a full cycle and a plurality of half cycle periods of an alternating current cycle.

12. (Original) A circuit as set forth in claim 1, wherein the timing circuit is a hysteresis circuit configured to produce pulses having a width corresponding to a predetermined period of time.

13. (Currently Amended) A circuit as set forth in claim 10, wherein the phase angle responsive circuit comprises:

a set/reset (S/R) flip flop circuit comprising:

first and second inverters, wherein the first inverter is configured to receive a gate signal which is produced in accordance with an alternating current that is supplied to the fusing system via the switch ~~drive~~ driver circuit, assuming a maximum voltage, and wherein the second inverter is configured to receive a zero cross signal when the voltage of the alternating current assumes a minimum value; and

first and second NAND logic gates wherein the first NAND logic gate is configured to receive the output of the first inverter and the output of the second NAND logic gate and wherein the second NAND logic gate is configured to receive the output of the second inverter and the output of the first NAND logic gate.

14. (Currently Amended) A circuit as set forth in claim 10, wherein the phase angle responsive circuit comprises a monostable circuit wherein [[the]] a trigger and reset terminals respectively receive a gate signal and a zero cross signal, the gate signal being produced in accordance with an alternating current which is supplied to the fusing system via the switch ~~drive~~ driver circuit, assuming a maximum voltage and the zero cross signal being produced in accordance with the alternating current assuming a minimum voltage.

15. (Currently Amended) A circuit for controlling the supply of alternating current to a fusing system including a fuser, comprising:

a fuser temperature sensor configured to produce a first output signal representative of the temperature of the fuser;

a temperature set point circuit configured to produce a second output signal representative of the temperature to which the fuser is to be heated;

a control circuit configured to be responsive to the first and second output signals, to monitor the temperature of the fusing system and to generate at least one control signal indicative that power should be supplied to the fuser;

a timing circuit configured to be responsive to the at least one control signal to generate a timing signal which determines the timing with which power should be supplied to the fuser; and

an averaging circuit configured to be responsive to the timing signal and to output a signal which gradually increases and decreases and which is used to control delivery of power to the fuser.

16. (Original) A circuit as set forth in claim 15, further comprising an opto isolator configured to be connected between the timing circuit and the averaging circuit and to electrically isolate the timing circuit from the averaging circuit.

17. (Original) A circuit as set forth in claim 15, further comprising a frequency modulation circuit configured to receive an output from the averaging circuit; and

a switch drive circuit configured to be responsive to the frequency modulation circuit and to supply alternating current to the fusing system.

18. (Original) A circuit as set forth in claim 17, wherein the frequency modulation circuit comprises a pulse width modulator (PWM) circuit.

19. (Original) A circuit as set forth in claim 17, wherein the frequency modulation circuit comprises a voltage controlled oscillator and a serially connected resetable monostable multivibrator.

20. (Original) A circuit as set forth in claim 17, wherein the frequency modulation circuit comprises a comparator configured to receive a first input from the averaging circuit and a second input from a serially connected oscillator and ramp generator.

21. (Original) A circuit for controlling a fusing system which is configured for connection to a source of alternating current, comprising:

a switch drive circuit for connecting the fusing system with the source of alternating current;

a timing circuit which produces a pulse train; and

an averaging circuit responsive to the pulse train from the timing circuit and connected with the switch drive circuit via a frequency modulation circuit.

22. (Original) A circuit as set forth in claim 21, wherein the timing circuit comprises a circuit configured to be responsive to a gate signal indicative of the voltage of the alternating current assuming a maximum value and a zero cross signal indicative of the voltage of the alternating current assuming a minimum value.

23. (Original) A circuit as set forth in claim 21, wherein the timing circuit is configured to produce an integral half cycle signal based on a full wave and a plurality of half waves of the alternating current.

24. (Original) A circuit as set forth in claim 21, wherein the timing circuit is configured to produce a pulse train wherein the width of the pulse corresponds to a predetermined time period.